

Abstract

A semiconductor memory component such as a mask-programmable ROM component, has two memory cell
5 transistors adjacent to each other in one column of a
memory cell field. First and a second row-
select/potential-equalization lines are equidistant
from the two memory cell transistors and vertically
above a diffusion region, which is assigned to both
10 memory cell transistors. The first or the second row-
select/potential-equalization line can be connected
both to the word line of the first memory cell
transistor and to the word line of the memory cell
transistor of the second memory cell for equalizing the
15 potential with one of the two word lines.